

COM-1505SOFT INTEGRATED PSK MODEM VHDL source code overview / IP core

Overview

The COM-1505SOFT is a complete PSK modem written in VHDL, including PSK modulation, demodulation, convolutional error correction encoding and decoding, scrambling, HDLC framing, TCP-IP network interface and USB 2.0 interface. It is designed to be embodied within a single low-cost FPGA such as the Xilinx Spartan-6 LX45.

The entire **VHDL source code** is included.

Key features and performance:

- PSK (BPSK, QPSK, OQPSK) modulation
- Continuous mode operation (i.e. Burst mode is not supported)
- Convolution error correction, rates 1/2, 2/3, 3/4, 5/6 and 7/8.
- Overall performance: $2 \cdot 10^{-5}$ BER @ 4dB Eb/No for K=7 rate 1/2 FEC.
- Serial HDLC to transmit empty frames over the synchronous link when no payload data is available.
- V.35 scrambling to randomize the modulated data stream.
- Maximum encoded data rate of 25 Msymbols/s when using a 100 MHz FPGA processing clock.
- User interfaces:
 - Synchronous serial with elastic buffer or
 - GbE TCP-IP server
 - USB 2.0 FS/HS
- Demodulator performance:
 - BER: < 0.5 dB implementation losses w.r.t. theory
 - Programmable frequency acquisition range.

- Demodulator acquisition threshold (uncoded) Eb/No = 2dB

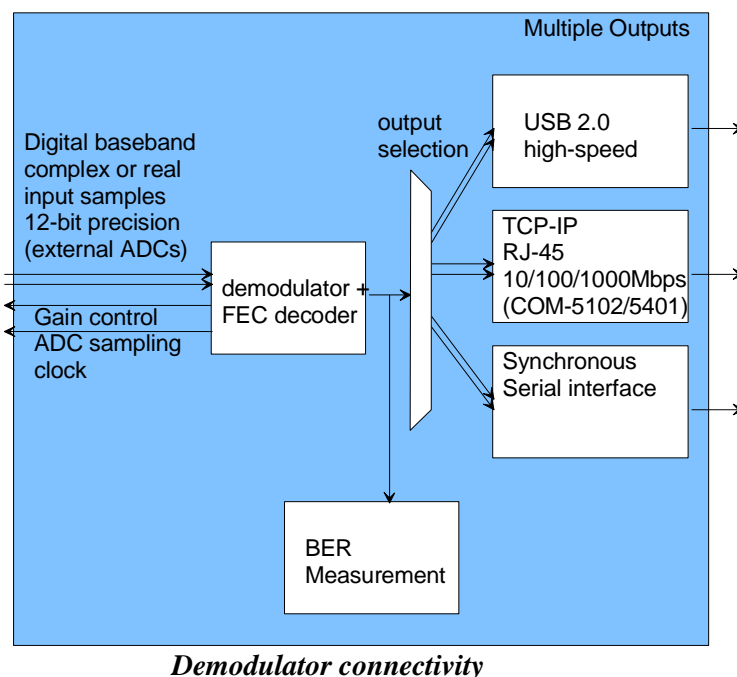
- Ancillary components are also included for streaming, test signal generation and bit error rate measurement.
- Drivers for the high-speed and auxiliary DACs and ADCs are included for a seamless interface with popular Analog Devices analog/digital converters

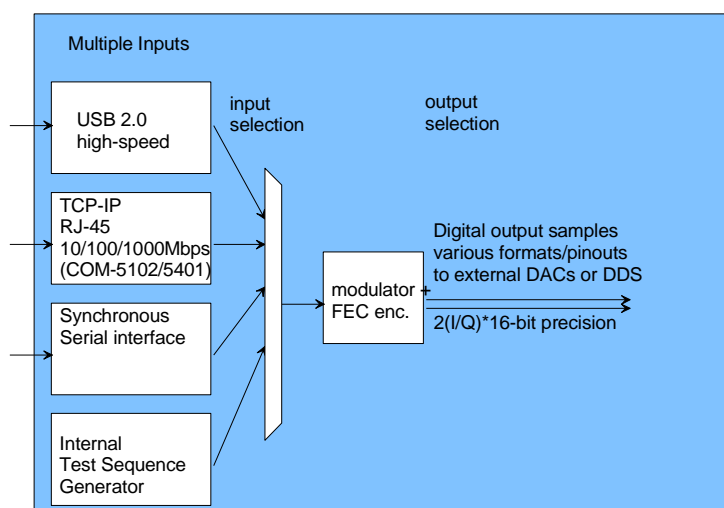
Target Hardware

The code is written in generic VHDL so that it can be ported to a variety of FPGAs. The code is developed and tested on a Xilinx Spartan-6 FPGA.

It can be easily ported to any Xilinx Kintex 7, Virtex-6, Virtex-5, Spartan-6 FPGAs and other FPGAs.

Overall Block Diagrams





Modulator connectivity

Synthesis-time configuration parameters

In the *COM1505.vhd* component, set the **OPTION** constant as

- A** for LAN and USB interfaces
- B** for synchronous serial (clk + data + cts) and USB interfaces
- C** for synchronous serial (clk + data), no HDLC.

Run-time configuration parameters

The user can set and modify the following controls at run-time through 8-bit control registers REGx, as listed below.

The baseline code is written so that control registers REGx are written by an external microcontroller through a simple 8-bit address/data bus. See process UC_WRITE_001.

Transmitter	
Parameters	Configuration
Input selection / format, test modes	<p>Select the origin of the transmitter input data stream.</p> <p>0 = high-speed USB, 8-bit parallel</p> <p>1 = LAN/TCP-IP, port 1024 (through Ethernet adapter), 8-bit parallel</p> <p>2 = 1-bit synchronous serial</p> <p>3 = internal PRBS-11 test sequence</p> <p>5 = unmodulated carrier</p> <p>8-bit parallel input bytes are transmitted MSb first.</p> <p>REG5(3:0)</p>

FEC convolutional encoder	
Parameters	Configuration
Constraint length K and rate R	<p>0001 = (K = 7, R=1/2, Intelsat)</p> <p>0010 = (K = 7, R=2/3, Intelsat)</p> <p>0011 = (K = 7, R=3/4, Intelsat)</p> <p>0100 = (K = 7, R=5/6, Intelsat)</p> <p>0101 = (K = 7, R=7/8, Intelsat)</p> <p>REG12(4:1)</p>
Differential Encoding	<p>Differential encoding is useful in removing phase ambiguities at the PSK demodulator, at the expense of doubling the bit error rate.</p> <p>When enabled, the differential decoding must be enabled at the receiving end.</p> <p>There is no need to use the differential encoding to remove phase ambiguities at the PSK demodulator when the Viterbi decoder and HDLC decoder are enabled.</p> <p>0 = disabled</p> <p>1 = enabled</p> <p>REG12(5)</p>
Bypass FEC encoding	<p>0 = encoding enabled</p> <p>1 = bypass</p> <p>REG12(6)</p>
V.35/Intelsat IESS 308 scrambling before FEC encoding	<p>0 = enabled</p> <p>1 = bypass</p> <p>REG12(7)</p>
PSK Modulator	
Parameters	Configuration
Processing clock f_{clk_tx}	<p>Modulator processing clock. Also serves as DAC sampling clock.</p> <p>20-bit unsigned integer expressed as $f_{clk_tx} * 2^{20} / 300MHz$.</p> <p>120 MHz maximum.</p> <p>20 MHz recommended minimum</p> <p>REG0 = bits 7-0 (LSB)</p> <p>REG1 = bits 15 – 8 (MSB)</p> <p>REG2(3:0) = bits 19 – 16 (MSB)</p>

Internal/External frequency reference	0 = internal. Use the internal 60 MHz clock (from the USB PHY) as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through the J7 SMA connector as frequency reference. REG2(7)
Symbol rate $f_{\text{symbol rate tx}}$	The modulator symbol rate is in the form $f_{\text{symbol rate tx}} = f_{\text{clk_tx}} / 2^n$ where n ranges from 1 ($f_{\text{clk_tx}}$ is twice the symbol rate) to 15 (symbol rate = $f_{\text{clk_tx}} / 65536$). n is defined in REG3(3:0)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK REG4(5:0)
Spectrum inversion	Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring in a subsequent RF frequency translation. 0 = off 1 = on REG4(6)
Channel filter enabled	0 = enable the spectrum shaping filters (root raised cosine, interpolation) 1 = bypass the spectrum shaping filters. (special use in applications when a root raised cosine filter is not used in the demodulator.) REG4(7)
Signal gain	Signal level. 16-bit unsigned integer. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend <u>checking for saturation at the D/A converter</u> when changing either the symbol rate or the signal gain. REG6 = bits 7-0 (LSB) REG7 = bits 15-8 (MSB)

Output Center frequency (f_{cout})	Frequency translation. 32-bit signed integer (2's complement representation) expressed as $f_{\text{cout}} * 2^{32} / f_{\text{clk_tx}}$ REG8 = bits 7-0 (LSB) REG9 = bits 15 – 8 REG10 = bits 23 – 16 REG11 = bits 31 – 23 (MSB)
Input bit rate	Option -C only Set the nominal input bit rate in order to generate a regular bit clock to the data source. Must be consistent with the modulator symbol rate, modulation type and FEC rate. Example: 2 Mbps : x051EB852 $f_{\text{input bit rate tx}} * 2^{32} / f_{\text{clk_rx}}$ REG13 = bits 7-0 (LSB) REG14 = bits 15 – 8 REG15 = bit 23 – 16 REG16 = bit 31 – 23 (MSB)
External transmitter gain control	When using an external transceiver such as the COM-350x family, the transmitter gain can be controlled through the TX_GAIN_CNTRL1 analog output signal. Range 0 – 3.3V. REG17 = bits 7-0 (LSB) REG18(3:0) = bits 11-8
External transmitter controls	REG19(0): TX_ENB REG19(1) = RX_TXN

Receiver	
PSK Demodulator	
Parameters	Configuration
Processing clock	<p>The demodulator processing clock also serves as A/D converter sampling clock.</p> <p>It can be generated within the FPGA or externally.</p> <p>Code baseline $f_{clk_rx} = 100$ MHz</p> <p>Note: when using IF undersampling, a dedicated oscillator is recommended as the FPGA-generated clock may show excessive jitter (which translates into phase noise).</p>
Nominal symbol rate $f_{symbol\ rate\ rx}$	<p>The demodulator nominal symbol rate is in the form $f_{symbol\ rate\ rx} * 2^{32} / f_{clk_rx}$</p> <p>REG25 = bits 7-0 (LSB)</p> <p>REG26 = bits 15 – 8</p> <p>REG27 = bit 23 – 16</p> <p>REG28 = bit 31 – 23 (MSB)</p>
Nominal Center frequency (f_{c_rx})	<p>Expected center frequency of the received signal. 32-bit signed integer (2's complement representation) expressed as $f_{c_rx} * 2^{32} / f_{clk_rx}$.</p> <p>In the case of IF undersampling, the residual intermediate frequency is removed here. For example, in the case of a 125 MHz IF signal sampled at 100 Msamples/s, the 25 MHz residual frequency is removed here by entering 0x40000000.</p> <p>REG29 = bit 7-0 (LSB)</p> <p>REG30 = bit 15 – 8</p> <p>REG31 = bit 23 – 16</p> <p>REG32 = bit 31 – 23 (MSB)</p>
Modulation type	<p>0 = BPSK</p> <p>1 = QPSK</p> <p>2 = OQPSK</p> <p>REG33(5:0)</p>

Spectrum inversion	<p>Invert Q bit. This is helpful in compensating any frequency spectrum inversion occurring during RF frequency translations.</p> <p>0 = off</p> <p>1 = on</p> <p>REG33(6)</p>
High SNR	<p>To minimize the false lock probability at high SNR, set this bit to '1' when Eb/No is likely to exceed 10dB. To emphasize operation at very low Eb/No, set this bit to '0'</p> <p>REG33(7)</p>
Frequency acquisition range (scan)	<p>The demodulator natural frequency acquisition range is around 1% of the symbol range (depending on modulation, SNR). The frequency acquisition range can be extended by frequency scanning. Scanning steps are spaced ($f_{symbol\ rate\ rx} / 512$) apart. The user can thus trade-off acquisition time versus frequency acquisition range by specifying the number of scanning steps here.</p> <p>For example, 52 steps yield a frequency acquisition range of $\pm(f_{symbol\ rate\ rx} * 0.10)$</p> <p>REG24</p>
AGC response time	<p>Users can to optimize the AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and symbol rate). The response time is approximately:</p> <p>0 = 8 symbols,</p> <p>1 = 16 symbols,</p> <p>2 = 32 symbols,</p> <p>3 = 64 symbols, etc....</p> <p>10 = every thousand symbols.</p> <p>Valid range 0 to 14.</p> <p>REG34(4:0)</p>
AGC internal / external	<p>0 = internal AGC</p> <p>1 = external AGC</p> <p>When selecting internal AGC mode, the user is responsible for avoiding saturation at or prior to the A/D converter.</p> <p>The internal AGC maximum gain is 256 in amplitude (48 dB in power). Therefore, it is recommended to keep the input samples amplitude between maximum and maximum/256. In the input dynamic range is larger, please adjust the INTERNAL_AGC_005 process within <i>RECEIVER1.vhd</i>.</p>

	REG34(7)
Input selection	<p>0 = digital real 12-bit unsigned samples, right connector, COM-3504 transceiver. Use in the case of IF input signal.</p> <p>1 = digital complex 2*12-bit unsigned samples, right connector, COM-3504 transceiver.. Use in case of baseband (near-zero center frequency) input signal.</p> <p>7 = internal loopback mode, from modulator.</p> <p>REG35(2:0)</p>
Viterbi FEC decoder	
Parameters	Configuration
Constraint length K and rate R	<p>0001 = (K = 7, R=1/2, Intelsat)</p> <p>0010 = (K = 7, R=2/3, Intelsat)</p> <p>0011 = (K = 7, R=3/4, Intelsat)</p> <p>0100 = (K = 7, R=5/6, Intelsat)</p> <p>0101 = (K = 7, R=7/8, Intelsat)</p> <p>REG37(4:1)</p>
Differential Decoding	<p>0 = disabled</p> <p>1 = enabled</p> <p>REG37(5)</p>
V.35/Intelsat IESS 308 descrambling after FEC decoding	<p>0 = enabled</p> <p>1 = bypass</p> <p>REG37(7)</p>
Bypass FEC decoding	<p>0 = decoding enabled</p> <p>1 = bypass</p> <p>REG38(7)</p>
Output selection	<p>0 = high-speed USB, 8-bit parallel</p> <p>1 = LAN/TCP-IP, port 1024 (through Ethernet adapter), 8-bit parallel</p> <p>2 = 1-bit synchronous serial</p> <p>3 = exclusively to the BER measurement</p> <p>REG36(2:0)</p>
Network Interface	
Parameters	Configuration
IP address (when connected to Gbit Ethernet PHY like COM-5102, COM-5104)	<p>4-byte IPv4 address.</p> <p>Example : 0x AC 10 01 80 designates address 172.16.1.128</p> <p>The new address becomes effective immediately (no need to reset the ComBlock).</p> <p>REG41: MSB</p> <p>REG42</p> <p>REG43</p> <p>REG44: LSB</p>

(Re-)Writing to the last control register REG44 is recommended after a configuration change to enact the change.

Configuration example 1

Modulator:

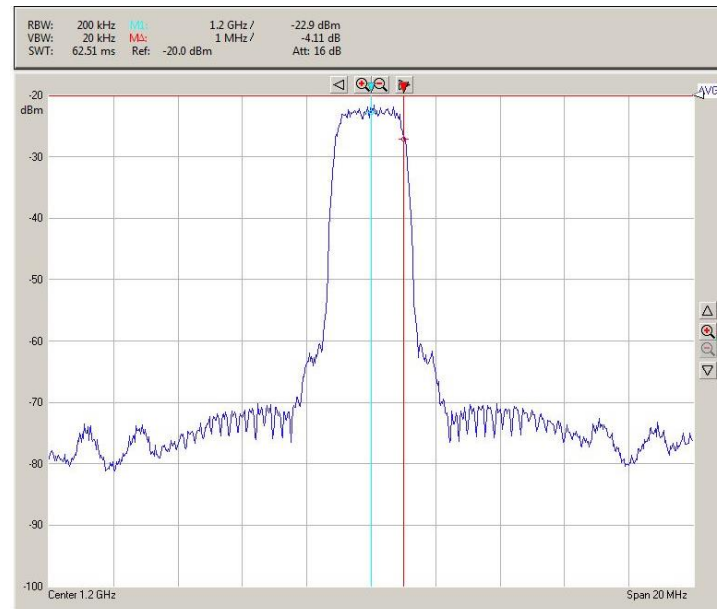
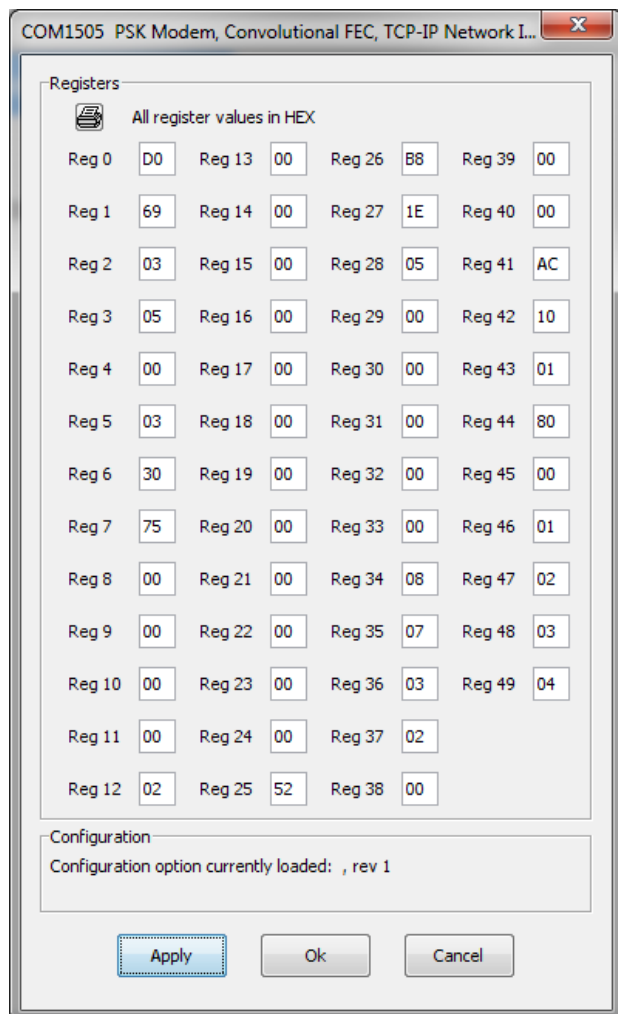
2 Msymbols/s modulation, BPSK, convolutional encoding $K=7$ $R=1/2$, PRBS-11 test sequence, baseband (0Hz) complex (I/Q) modulated output signal.

Demodulator:

2 Msymbols/s, BPSK, convolutional encoding $K=7$ $R=1/2$, internal AGC with response speed 8, internal loopback mode, demodulated data directly to BER measurement.

IP address 172.16.1.128

MAC address: 00 01 02 03 04 05



Typical RF output spectrum (after D/A conversion and direct RF modulation)

Configuration example 2

Modulator:

144 Ksymbols/s modulation, BPSK, convolutional encoding $K=7$ $R=1/2$, from LAN/TCP-IP, baseband (0Hz) complex (I/Q) modulated output signal.

Demodulator:

144 Ksymbols/s, BPSK, convolutional encoding $K=7$ $R=1/2$, internal AGC with response speed 8, internal loopback mode, demodulated data to LAN/TCP-IP

IP address 172.16.1.128

MAC address: 00 01 02 03 04 05

COM1505 PSK Modem, Convolutional FEC, TCP-IP Network I...

Registers

All register values in HEX

Reg 0	A2	Reg 13	00	Reg 26	5F	Reg 39	00
Reg 1	EE	Reg 14	00	Reg 27	5E	Reg 40	00
Reg 2	03	Reg 15	00	Reg 28	00	Reg 41	AC
Reg 3	09	Reg 16	00	Reg 29	00	Reg 42	10
Reg 4	00	Reg 17	00	Reg 30	00	Reg 43	01
Reg 5	01	Reg 18	00	Reg 31	00	Reg 44	80
Reg 6	30	Reg 19	00	Reg 32	00	Reg 45	00
Reg 7	75	Reg 20	00	Reg 33	00	Reg 46	01
Reg 8	00	Reg 21	00	Reg 34	08	Reg 47	02
Reg 9	00	Reg 22	00	Reg 35	07	Reg 48	03
Reg 10	00	Reg 23	00	Reg 36	01	Reg 49	04
Reg 11	00	Reg 24	00	Reg 37	02		
Reg 12	02	Reg 25	31	Reg 38	00		

Configuration

Configuration option currently loaded: , rev 1

Apply Ok Cancel

Configuration example 3

Same as above with 70 MHz IF input (requires an external anti-aliasing bandpass filter)

Set REG32/31/30/29 to B3 33 33 33 (-30 MHz).

Status Registers

The baseline code is written so that 8-bit status registers SREGx are read by an external microcontroller through an 8-bit address/data bus. See process UC_READ_001.

Digital status registers are read-only.

PSK/QAM/PSK Demodulator Monitoring	
Parameters	Monitoring
Front-end AGC	8-bit unsigned value prior to DAC conversion to RX_AGC1. Inverted scale: 0 is for the maximum gain. SREG10
Carrier frequency offset (fcdelta)	Residual frequency offset with respect to the nominal carrier frequency. 24-bit signed integer (2's complement) expressed as $fcdelta * 2^{24} / f_{clk_rx}$. SREG11 = LSB SREG12 SREG13 = MSB
Carrier tracking loop lock status	Lock is declared if the standard deviation of the phase error is less than 25deg rms. 0 = unlocked 1 = locked SREG14(0)
Inverse SNR	A measure of noise over signal power. 0 represents a noiseless signal. Valid only when demodulator is locked. SREG15
Viterbi FEC decoder monitoring	
Parameters	Monitoring
Synchronized	(FEC_DEC_LOCK_STATUS variable) Solid '1' when the Viterbi decoder is locked. '0' or toggling when unlocked. SREG14(1)
Decoder built-in BER	The Viterbi decoder computes the BER on the received (encoded) data stream irrespective of the transmitted bit stream. Encoded stream bit errors detected over a 1000-bit measurement window (unless modified in <i>com1509pkg.vhd</i>). SREG16 = bits 7 – 0 (LSB) SREG17 = bits 15 – 8 SREG18 = bits 23 – 16 (MSB)

HDLC decoder monitoring	
Parameters	Monitoring
Cumulative number of valid bits at HDLC output	SREG19: LSB SREG20: SREG21: SREG22: MSB
BER Measurement	
Parameters	Monitoring
Bit Errors	<p>Bit errors can be counted when a PRBS-11 test sequence is transmitted.</p> <p>Number of bit errors in a 1,000,000 bit window. 32 bit unsigned. SREG23: error_count[7:0] (LSB) SREG24: error_count[15:8] SREG25: error_count[23:16] SREG26: error_count[31:24] (MSB)</p> <p>The bit errors counter is updated once every periodic measurement window. Reading the value will not reset the counter.</p>
BER Synchronization status	<p>0 = not synchronized. 2047-bit pattern is not detected.</p> <p>1 = synchronized SREG27(0)</p>
TCP-IP Connection Monitoring	
Parameters	Monitoring
TCP-IP connection on port 1024 (data stream)	<p>Bit 0 = port 1028 (M&C) connected Bit 1 = port 1024 (data) connected 1 for connected, 0 otherwise SREG28(1:0)</p>
LAN PHY ID	<p>Expect 0x22 when the PHY IC is Micrel KSZ9021. SREG29(LSB)</p>
MAC address	<p>Unique 48-bit hardware address (802.3). In the form SREG30:SREG31:SREG32:....:SREG35</p> <p>Since the MAC address is unique, it can also be used as a unique identifier in a radio network with many nodes.</p>

Note: multi-words status registers such as frequency offset or BER, are latched upon reading status register SREG10.

Troubleshooting checklist

1. Place modem in loopback mode (REG35 = 0x07) while sending a PRBS-11 test sequence (REG5 = 0x03). Be sure to direct the demodulated bit stream to the BER measurement (REG36 = 0x03).

Check the status registers for

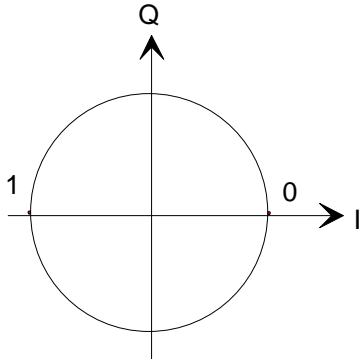
- a. Demodulator and Viterbi decoder are locked:
SREG14 = 0x03
- b. No Viterbi decoder errors:
SREG16/17/18 = 0
- c. BER measurement is synchronized:
SREG27 = 0x01
- d. No BER errors:
SREG23/24/25/26 = 0
- e. Bits are being received at the HDLC decoder output:
SREG19/20/21/22 counter keeps increasing at a rate consistent with the modulation rate.

Operation

Constellation: Symbol Mapping

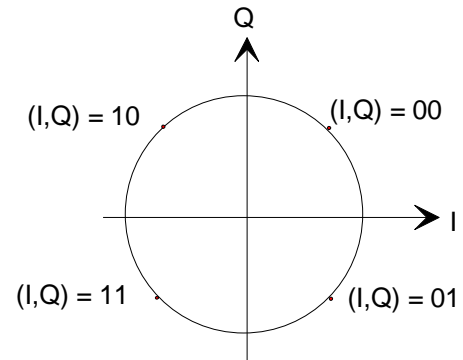
The packing of serial data stream into symbols is done with the Most Significant bit first.

BPSK

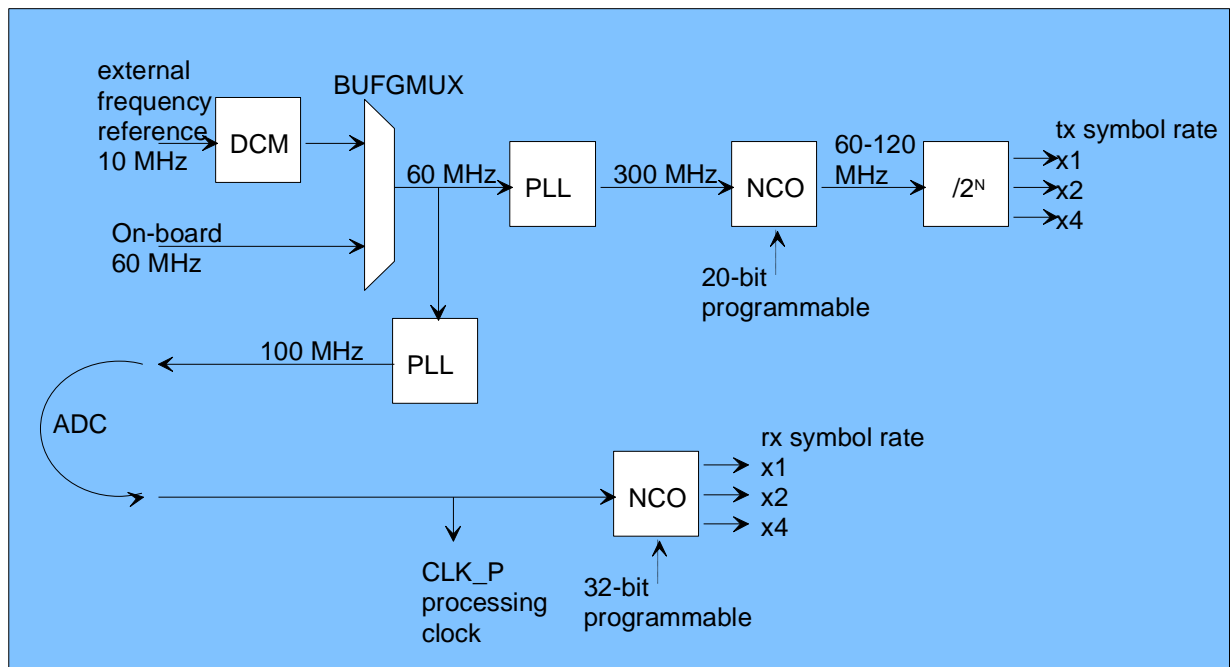


QPSK

Gray encoding.



Clocks generation



The software is written to accept a 10 MHz or a 60 MHz clock as frequency reference.

The design includes several clock domains:

CLK_P: main processing clock (selected to be the same as the ADC sampling clock in this project).

CLK_TXG: processing clock for the digital PSK modulator. This clock is programmable (see control registers REG0 through REG2) as it relates to the modulation symbol rate: it is always a power of 2 multiple of the modulation symbol rate. 60 to 120 MHz for a Xilinx Spartan-6 implementation.

USB_CLK60G: processing clock for the USB 2.0 serial interface engine. Always 60 MHz. Supplied by the external USB PHY through the standard ULPI interface.

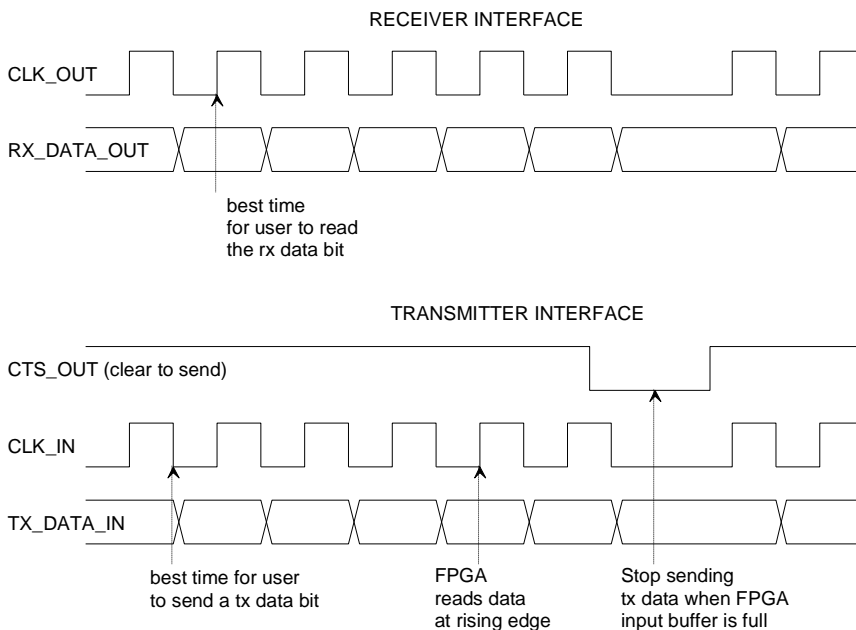
LAN1_RXC: 2.5/25/125 MHz clock for the 10/100/1000 Ethernet MAC (COM5401.vhd). Supplied by the external LAN PHY through the standard RGMII interface.

Limitation and trade-off: Due to the lack of flexible programmable PLL in the Xilinx Spartan-6 family, we use an ad-hoc high-speed NCO which is quite flexible (20-bit precision) but which is afflicted by 3ns peak-peak jitter. To mitigate this impairment, the modulated signal is resampled and filtered, creating some minor aliasing (-45 dB).

Substituting the HIGH_SPEED_NCO.vhd component with the DCM_CLKGEN_DYNAMIC.vhd component eliminates the aliasing impairments but limits the symbol rate programmability to coarser steps of at most 1% (versus 3ppm for the baseline version).

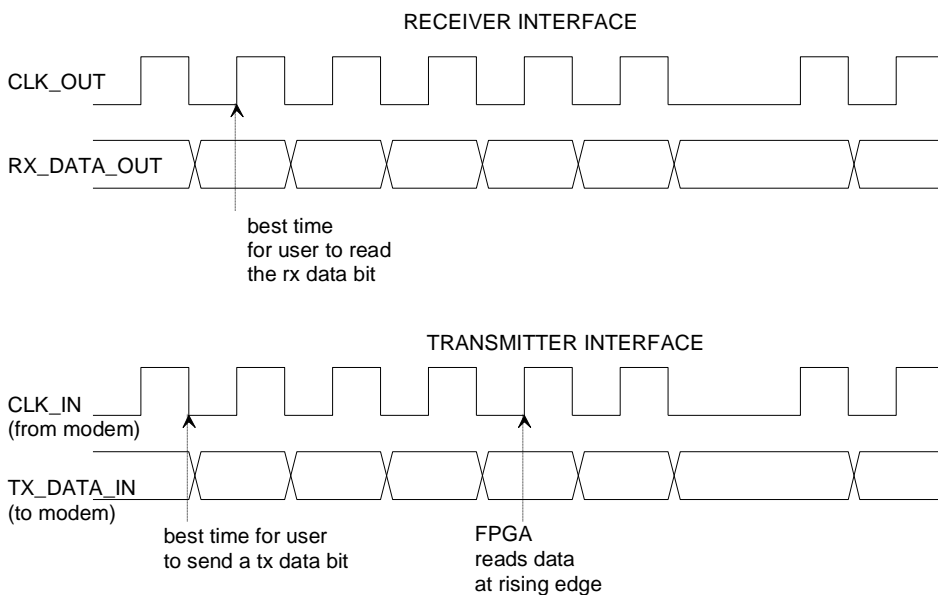
I/Os

1-bit synchronous serial (-B option)



In the transmit direction, the user provides both clock (CLK_IN) and data (TX_DATA_IN). The user should always check the “Clear-To-Send” CTS_OUT flag before sending additional data bits to the modulator. As option **-B** includes HDLC, the user is allowed not to transmit data. When so, the modem will send empty HDLC frames.

1-bit synchronous serial (-C option)



In the transmit direction, the user provides serial data (TX_DATA_IN), preferably at the falling edge of the modem-supplied CLK_IN. The TX_DATA_IN is read at the rising edge of CLK_IN. The user **MUST** provide data, otherwise an underflow condition will occur. Option **-C** is for continuous-mode operation. No gap in data

transmission is allowed.

TCP-IP (-A option)

The transmit and receive data streams can also be transferred over a TCP-IP network connection. This requires an additional Ethernet PHY with standard RGMII or GMII interface (a COM-5102 plug-in Ethernet adapter for example).

In this case, the modem acts as a TCP server, waiting for connection from a remote client at port 1024. A unique IP address and a unique MAC address must be assigned to the modem (see control registers REG41 through REG50).

The TCP-IP protocol guarantees that no overflow will occur in the user to modem direction. The built-in flow-control mechanism of the TCP-IP will prevent the user application from writing more data than the modem can handle for the specified data rate.

In the receiver to user direction however, it is the user's responsibility to read data as fast as possible to prevent an overflow condition from occurring at the receiver.

The TCP bytes are sent/received serially, most-significant bit first.

The modem monitoring and control information can also be sent over the same physical link, using the TCP server at port 1028.

More information regarding the built-in 10/100/1000 Mbps Ethernet MAC and the TCP server can be found here:

www.comblock.com/download/com5401soft.pdf

www.comblock.com/download/com5402soft.pdf

USB

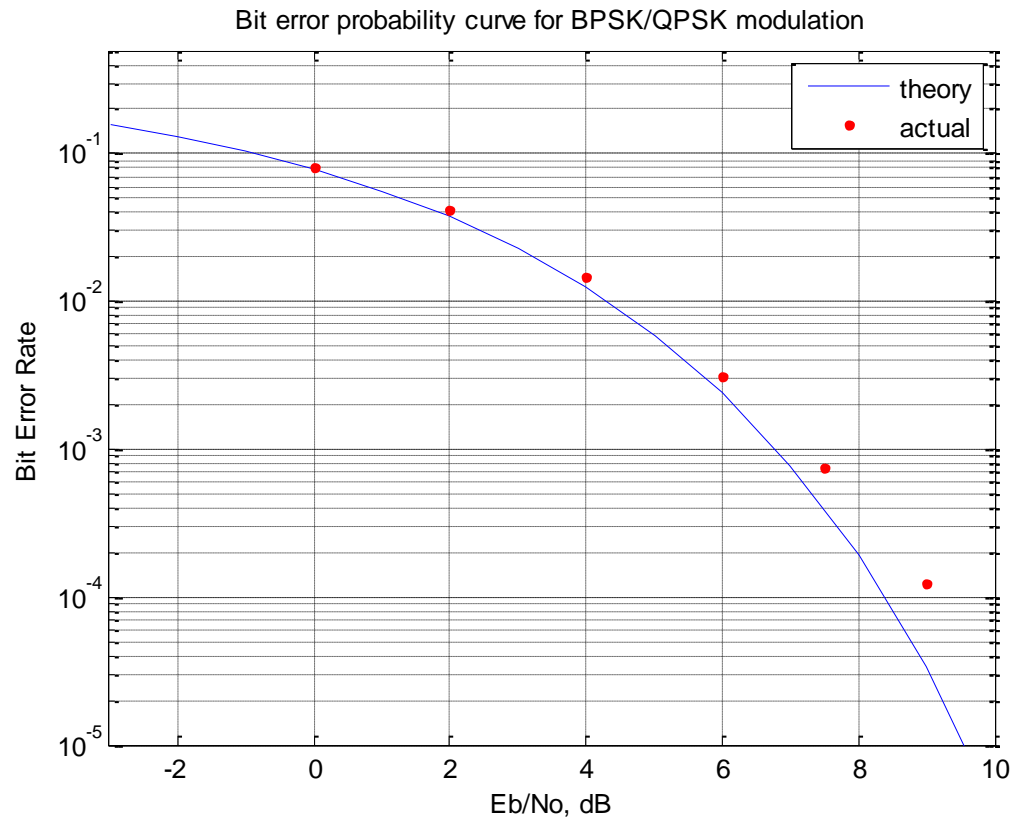
Data streams can also be transmitted over a USB 2.0 cable, together with monitoring and control information. This modem acts as a USB device.

See http://comblock.com/download/USB20_UserManual.pdf for details.

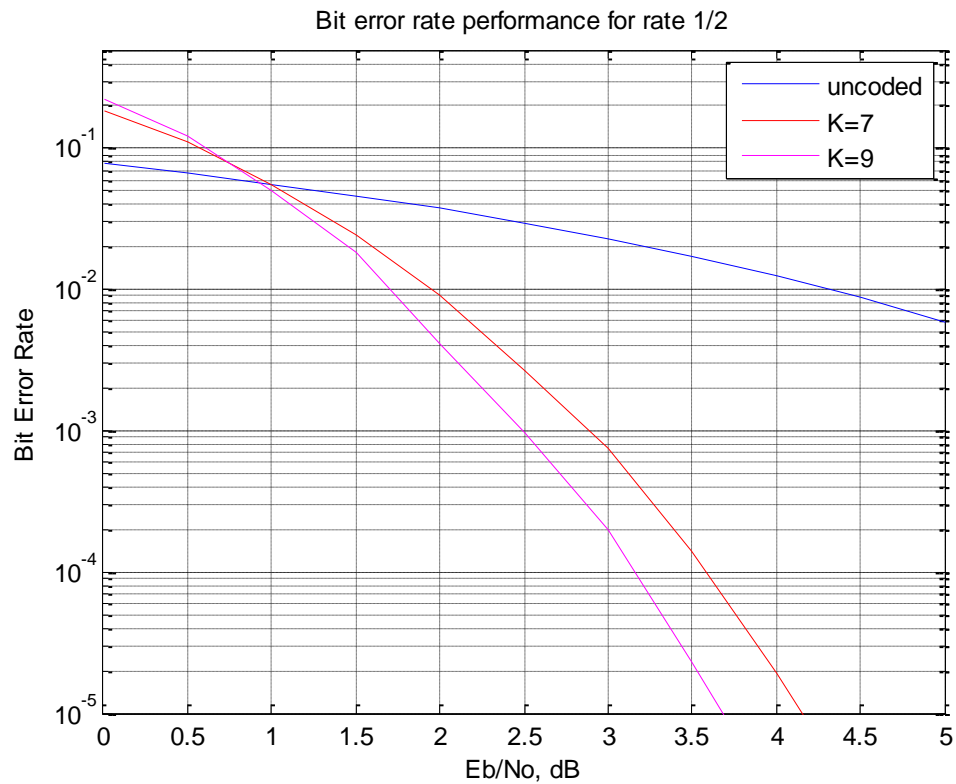
More information regarding the built-in USB 2.0 Serial Interface Engine (SIE) can be found here:

<http://comblock.com/download/USB2soft.pdf>

Performance

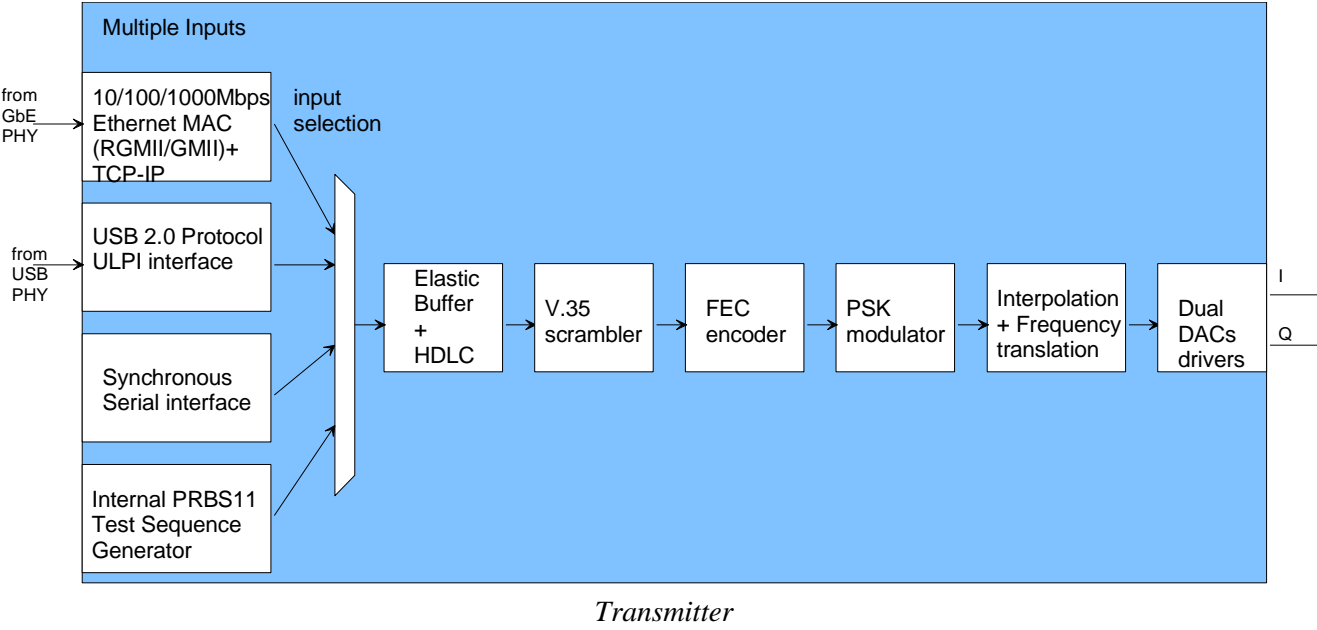
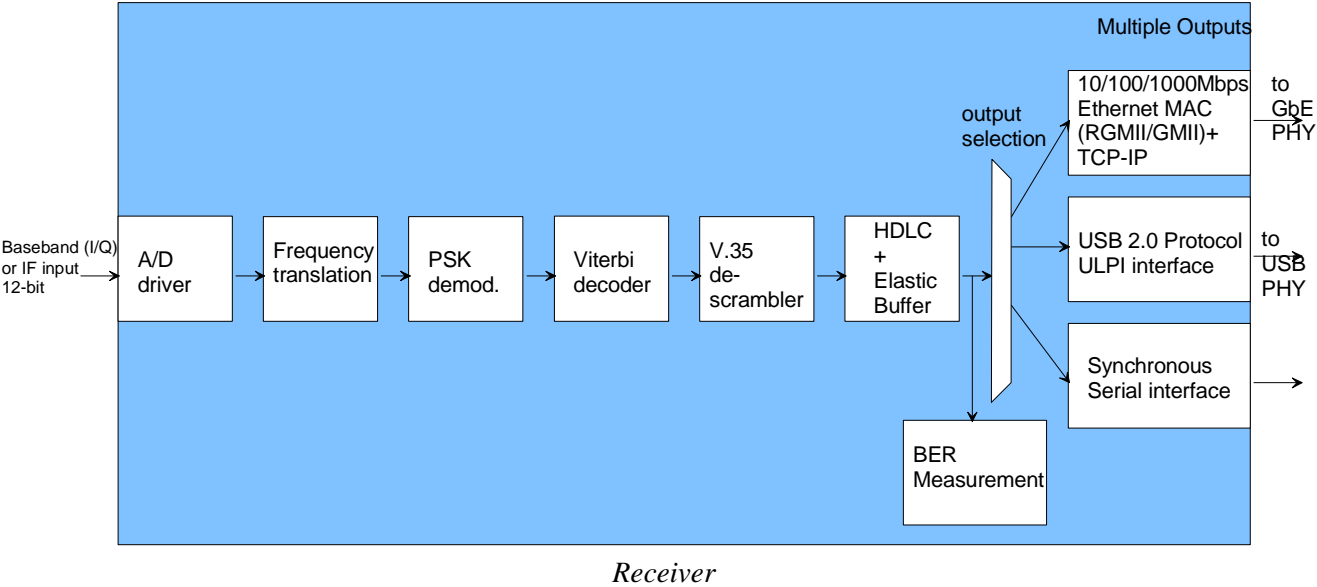


BER performance, demodulator only (no FEC)



BER performance, FEC only (no demodulator)

Implementation Block Diagram



Software Licensing

The COM-1505SOFT is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bitstream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from <http://www.comblock.com/download/softwarelicense.pdf>

Configuration Management

The current software revision is 2.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code, .ucf constraint files, .pkg packages. One component per file.
/sim	Test benches, Matlab .m signal generation program
/bin	.ngc, .bit, .mcs configuration files

Key files:

Xilinx ISE project file: com-1505_ISE431.xise

.ucf constraint file example when used on the COM-1500 FPGA platform:

\src\COM1505.ucf

VHDL development environment

The VHDL software was developed using the following development environment:

- (a) Xilinx ISE 14.1 with XST as synthesis tool
- (b) Xilinx ISE Isim as VHDL simulation tool

The entire project fits within a Xilinx Spartan-6 LX45. Therefore, the ISE project can be processed using the free Xilinx WebPack tools.

Device Utilization Summary

Device: Xilinx Spartan-6

OPTION-A LAN and USB interfaces		% of Spartan-6 LX45
Registers	17271	31%
LUTs	1887	69% 1
Block RAM	44	37%
DSP48A1s	30	48%
GCLKs	10	62%
DCMs	3	37%
PLL_ADVs	2	50%
OPTION-B Synchronous serial and USB interfaces		% of Spartan-6 LX45
Registers	14154	25%
LUTs	15089	55%
Block RAM	25	21%
DSP48A1s	24	41%
GCLKs	8	50%
DCMs	3	37%
PLL_ADVs	2	50%
OPTION-C synchronous serial (clk + data), no HDLC		% of Spartan-6 LX45
Registers	14484	26%
LUTs	15039	55%
Block RAM	26	22%
DSP48A1s	30	51%
GCLKs	9	56%
DCMs	3	37%
PLL_ADVs	2	50%

Clock and modem speed

The modem design primarily uses two global clocks: a transmit DAC clock and a receive ADC clock. Typical maximum clock frequencies for various FPGA families are listed below:

Device family	CLK_RXG	CLK_TXG	Max. symbol rate
Xilinx Kintex 7 -2			
Xilinx Virtex-	100 MHz	120 MHz	25 MS/s

6-2			
Xilinx Spartan-6 -3			

Ready-to-use Hardware

The COM-1505SOFT was developed on, and therefore ready to use on the following commercial off-the-shelf hardware platform:

FPGA development platform
COM-1500 FPGA + DDR2 SODIMM socket + ARM development platform
Network adapter
COM-5102 Gigabit Ethernet + HDMI interface
Analog
COM-3504 Dual Analog <-> Digital Conversions

Xilinx-specific code

The VHDL source code is written in generic VHDL with few Xilinx primitives. No Xilinx CORE is used. The Xilinx primitives are:

- IBUF
- IBUFG
- BUFG (global clocks)
- PLL_BASE (clock generation)
- DCM (clock generation)
- RAM block
- MULT18X18 hardware multiplier

VHDL components overview

Top level



COM1505.vhd: top level. Includes modulator, demodulator, clock generation, interface to a supervisory microcontroller (8-bit address/data bus to exchange control registers REG and status registers SREG). CLK_P is the main processing clock.

LFSR11P.vhd: pseudo random binary sequence generator PRBS-11. 8-bit parallel output for a maximum data rate of 8 times the processing clock frequency.

HDLC_SERIAL_2TX.vhd: bit-serial HDLC is used for asynchronous to synchronous conversion. The components inserts empty frames to tell the destination when no data is being transmitted over the synchronous (always on) link. It encapsulates payload data within frames of at most 512 bytes. A shorter frame will be transmitted over the link if no new payload data is available within 20us. A 16-bit CRC is appended to each non-empty frame to detect and reject erroneous frames at the receiving end. The matching component at the receiving end is *HDLC_SERIAL_2RX.vhd*.

V35SCRAMBLER.vhd implements ITU V.35 (Intelsat IESS-308) scrambling or descrambling.

Scrambling is required to randomized the transmitted data stream before FEC encoding.

ENCODER_ROOT.vhd: convolutional encoder. The matching component at the receiving end is *VITERBI_DECODER.vhd*.

Bit serial to 8-bit parallel conversions and back are implemented by *PX_TO_P8_CONVERSION.vhd* and *P8_TO_S1_CONVERSION.vhd* respectively.

CROSS_CLK_DOMAINS_NODATALOSS.vhd preserves the signal integrity while crossing clock domains (from the general processing clock domain CLK_P to the digital modulator clock domain CLK_TXG for example).

BURST_MODULATOR.vhd implements the digital modulation and spectrum shaping. Key controls include modulation symbol rate, output signal amplitude, modulation type (BPSK., QPSK, etc). The programmable modulation symbol rate sets the entire transmitter data throughput.

RECEIVER1.vhd is the front-end digital receiver which processes digital samples from the A/D converter(s). Its functions include fixed frequency translation to (near-zero) baseband, AGC, variable decimation (CIC) filters and one half-band filter for image rejection. Input digital samples can be complex (in the case of baseband input samples) or real (in the case of IF undersampling).

PSK_DEMOD2.vhd demodulates the PSK symbols while tracking the received modulated signal three key parameters: amplitude, center frequency and symbol rate.

BER2.vhd synchronizes with the received bit stream and counts the number of bit error when a PRBS-11 sequence is being transmitted.

USB20ULPI.vhd implements the USB 2.0 protocol Serial Interface Engine. It acts as a driver for an external USB PHY integrated circuit through a standard ULPI low pin interface.

COM5401.vhd implements the 10/100/1000 Ethernet MAC functions. It is designed to interface with an external Gigabit Ethernet PHY integrated

circuit via a standard RGMII or GMII interface. The default interface is RGMII. [\[1\]](#)

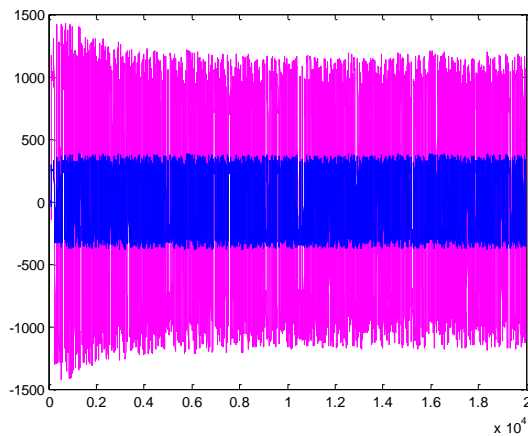
COM5402.vhd implements the higher-level IP protocols, namely ARP, PING, TCP server, UDP. Two TCP servers are configured by default: at port 1024 for payload transmit and receive, at port 1028 for monitoring and control. From the network, the modem is a TCP server: it listens for a remote connection from a client before transferring data. [\[2\]](#)

Receiver simulation

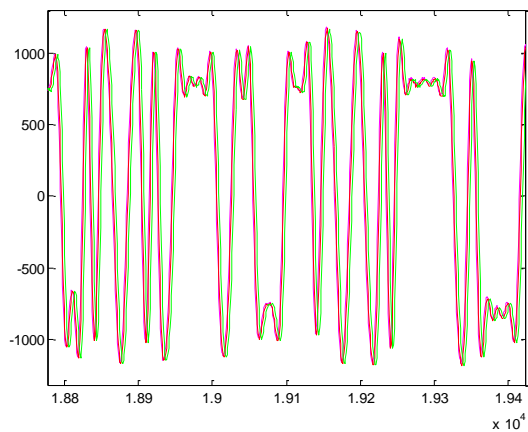
The internal digital signal processing can be illustrated by the following screenshots obtained through VHDL simulation. A Matlab program (siggen_psk2.m) generates a stimulus file which mimics A/D converter samples at the receiver input.

Internal FPGA signals are saved into Matlab loadable (load command) text files by setting the constant SIMULATION to '1' in various VHDL components.

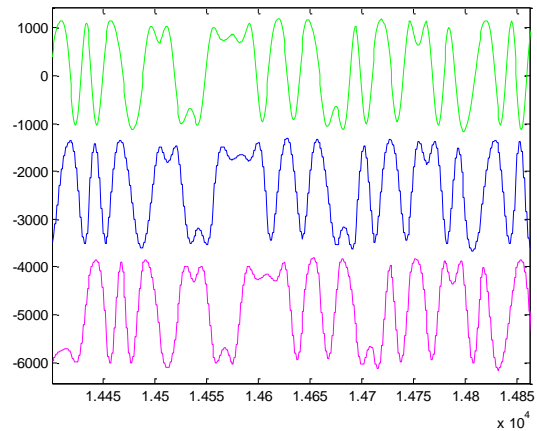
Ideal signals case: 100 Msamples/s input samples, 10 Msymbol/s BPSK modulation, 20% rolloff, no impairments (noiseless channel, no symbol timing error, no center frequency error).



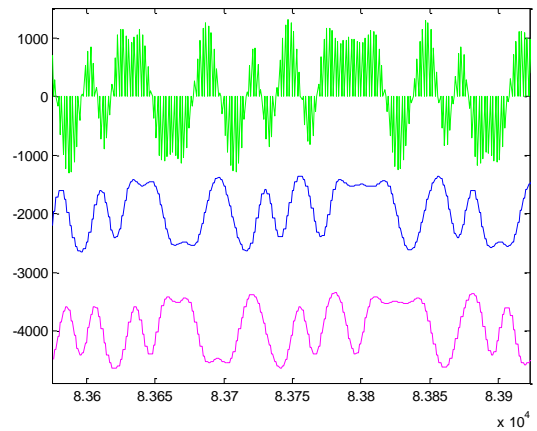
receiver1.vhd: input I-channel (blue), after internal AGC normalization (magenta).



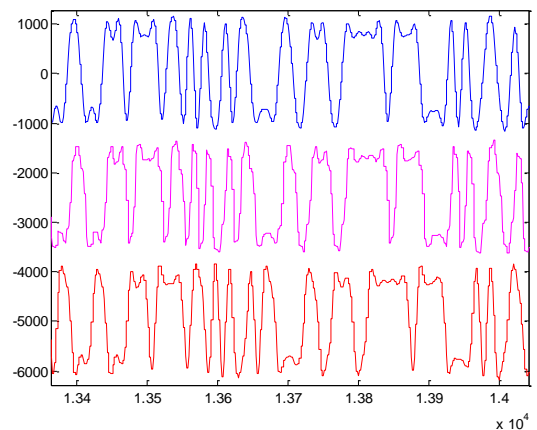
receiver1.vhd: after internal AGC normalization (magenta), bias removal (red) and frequency translation to baseband (green). [ideal case: no bias, no frequency error]



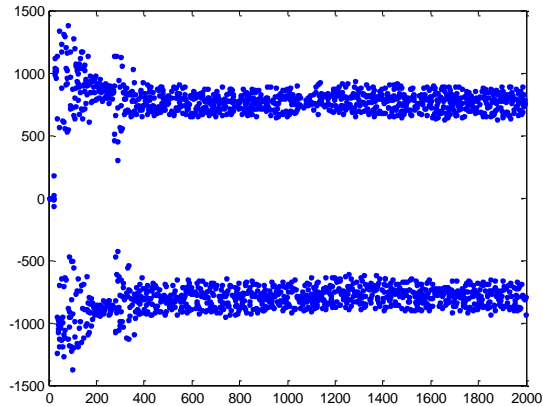
receiver1.vhd, baseband input case: after frequency translation to baseband (green), CIC decimation (blue) and half-band filter (magenta)



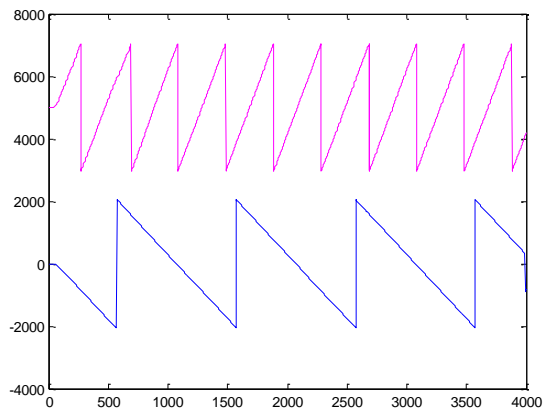
receiver1.vhd: illustrating frequency translation from IF input to baseband: after frequency translation to baseband (green), CIC decimation (blue) and half-band filter (magenta)



psk_demod2.vhd: after phase correction (blue), resampling at 4 samples/symbol (magenta), half-band low-pass filtering (red)



psk_demod2.vhd: after root raised cosine filter, subsampled at 1 sample per symbol (center of the eye diagram). Shows the symbol timing tracking loop convergence at start-up.



psk_demod2.vhd: carrier tracking, phase replica for -50KHz (magenta) and +20KHz (blue) frequency error.

Reference documents

[1] COM-5401SOFT Tri-mode 10/100/1000 Ethernet MAC, VHDL source code overview

www.comblock.com/download/com5401soft.pdf

[2] COM-5402SOFT

IP/TCP/UDP/ARP/PING STACK for GbE

VHDL source code overview

www.comblock.com/download/com5402soft.pdf

ComBlock Ordering Information

COM-1505SOFT INTEGRATED PSK MODEM

Contact Information

MSS • 18221-A Flower Hill Way •
Gaithersburg, Maryland 20879 • U.S.A.

Telephone: (240) 631-1111

Facsimile: (240) 631-1676

E-mail: info@comblock.com